WHAT IS CLAIMED IS:

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      1. A data input circuit converting input serial data to n-bit parallel data, and outputting the n-bit parallel data by following an address signal, said data input circuit comprising:

10   a data shifting unit including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and

      a selection unit selecting a column among the plurality of columns as an input column by

15 following the address signal, wherein the input serial data is inputted to said data shifting unit through the input column.

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      2. The data input circuit as claimed in claim 1, wherein said data shifting unit includes 2n-1 columns, and said selection unit selects the

25 input column through which the input serial data is inputted to said data shifting unit.

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      3. The data input circuit as claimed in claim 2, wherein said data shifting unit executes a logical arithmetic operation on a combination of outputs of n columns storing the input serial data

35 and outputs of n-1 columns not storing the input serial data, thereby converting the input serial data to the n-bit parallel data following the

address signal.

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4.   The data input circuit as claimed in claim 1 wherein:

said data shifting unit includes n columns, and a feed-back function feeding the input serial

10   data stored in a n'th column of said data shifting unit back to a first column of said data shifting unit; and

said selection unit selects the input column by following the address signal so as to

15   input the input serial data to said data shifting unit.

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5.   The data input circuit as claimed in claim 4, wherein said data shifting unit converts the input serial data to the n-bit parallel data following the address signal by outputting the input

25   serial data from the n columns storing the input serial data.

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6.   The data input circuit as claimed in claim 1 wherein, said input serial data is inputted by n bits to said data shifting unit, and a destination of each bit is determined by the address

35   signal.

7.   The data input circuit as claimed in claim 1, wherein:

said data shifting unit includes a plurality of data storage units as the plurality of
5   columns, and a plurality of switching units controlled by said selection unit, said plurality of data storage units storing the input serial data; and

said selection unit selects a data storage
10   unit as the input column among the plurality of data storage units by controlling the plurality of switching units.

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8.   A semiconductor device including a data input circuit converting input serial data to n-bit parallel data, and outputting the n-bit
20   parallel data by following an address signal, said semiconductor device comprising:

a data shifting unit including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and
25   a selection unit selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting unit through the input column.

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9.   The Semiconductor device as claimed
35   in claim 8, wherein:

said data shifting unit includes a plurality of data storage units as the plurality of

columns, and a plurality of switching units controlled by said selection unit, said plurality of data storage units storing the input serial data; and

5   said selection unit selects a data storage unit as the input column among the plurality of data storage units by controlling the plurality of switching units.

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        10.   A method of converting input serial data to n-bit parallel data, and outputting the n-
15   bit parallel data by following an address signal, said method comprising the steps of:
        selecting a column among a plurality of columns of a data shifting unit as an input column by following the address signal;
20   inputting the input serial data to said data shifting unit through the input column; and
        shifting the input serial data sequentially through the plurality of columns.